REMARKS

At the outset, Applicants request an interview to advance prosecution.

In the Final Office Action, the Examiner rejected claims 1-8, 11-17, 35-38, and 41-46 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,832,265 to Ma et al. (Ma) in view of U.S. Patent No. 7,385,997 to Gorti et al. (Gorti) and U.S. Patent Publication No. 2003/0169757 to LaVigne et al. (LaVigne); and rejected claims 9, 10, 39, and 40 under 35 U.S.C. § 103(a) as unpatentable over Ma, Gorti, LaVigne, and U.S. Patent 6,789,056 to Vinnakota.

By this amendment, Applicants amends claims 1, 2, 35, and 46 to more clearly claim the features of those claims.

Claims 1-17 and 35-46 are currently pending in the application.

The Examiner rejected claims 1-8, 11-17, 35-38, and 41-46 under 35 U.S.C. § 103(a) as unpatentable over Ma, Gorti, and LaVigne. Applicants respectfully traverse this rejection.

Amended claim 1 recites a combination including:

> allocating each received packet, based on priority information in the received packet, to at least one arrival queue of a plurality of arrival queues, wherein each of the plurality of arrival queues handles packets based on a traffic class associated with a priority, wherein each received packet comprises an internet protocol packet;
>
> placing each packet in the allocated arrival queue if said arrival queue is not full, otherwise dropping said packet;
>
> scheduling, by a scheduler coupled to the at least one arrival queue, packets from the arrival queue to at least one transfer queue;
>
> responsive to transfer of a packet to a transfer queue, generating an interrupt;
>
> responsive to receipt of an interrupt, allocating the packet from said transfer queue to one of a plurality of processor queues;
>
> placing the packet in the allocated processor queue if said processor queue is not full, wherein the at least one transfer queue and the at least one processor queue do not drop packets, and wherein the scheduler inhibits

placement of the packet when the processor queue is full to prevent dropping the packet; and

scheduling packets from the processor queues to be processed, wherein the at least one arrival queue, the at least one transfer queue, and the plurality of processor queues are separate queues, wherein the scheduler includes a first quantity N of inputs each corresponding to the at least one arrival queue, the scheduler further including a second quantity M of outputs each corresponding to the at least one transfer queue, wherein the second quantity M is less than or equal to the first quantity N.

Ma discloses moving packets within a device, such as a router. Specifically, rather than use a traditional round robin approach to move packets from receive queues 32 to transmit queues 36, Ma discloses using a modified round robin that services the "hungriest" interfaces first. Ma further describes using a controller 108 that loops through interfaces based on weights assigned to the interfaces to take into account the interfaces which are hungriest, i.e., "have more capacity for transmitting data." Ma at col. 10, lines 37-42. Because Ma uses a controller that merely moves packets from the receive queue to the transmit queue based on weights, it is not surprising that Ma does not disclose a scheduler. Indeed, nowhere does Ma disclose a scheduler. For at least this reason, Ma fails to disclose or suggest at least the following feature of claim 1: "scheduling, by a scheduler coupled to the at least one arrival queue, packets from the arrival queue to at least one transfer queue;" and "placing the packet in the allocated processor queue if said processor queue is not full, wherein the at least one transfer queue and the at least one processor queue do not drop packets, and wherein the scheduler inhibits placement of the packet when the processor queue is full to prevent dropping the packet."

Moreover, Ma merely moves packets from the receive queue to the transmit queue in a loop-like manner based on the "weights," giving priority to interrupts which

are perceived as hungrier. Thus, Ma handles packets without any regard to the priority of the packet itself. Therefore, Ma fails to disclose or suggest "allocating each received packet, based on priority information in the received packet, to at least one arrival queue of a plurality of arrival queues, wherein each of the plurality of arrival queues handles packets based on a traffic class associated with priority, wherein each received packet comprises an internet protocol packet."

Furthermore, Ma handles packets based on a looping, round robin scheme which takes into account the hungrier interfaces. But Ma moves a packet from a receive queue to an output queue with the capacity to handle the packet. Thus, it is not surprising that Ma is completely silent with regard to how to handle dropped packets, much less the following features of claim 1: "placing each packet in the allocated arrival queue if said arrival queue is not full, otherwise dropping said packet; scheduling, by a scheduler coupled to the at least one arrival queue, packets from the arrival queue to at least one transfer queue; responsive to transfer of a packet to a transfer queue, generating an interrupt; responsive to receipt of an interrupt, allocating the packet from said transfer queue to one of a plurality of processor queues; [and] placing the packet in the allocated processor queue if said processor queue is not full, wherein the at least one transfer queue and the at least one processor queue do not drop packets, and wherein the scheduler inhibits placement of the packet when the processor queue is full to prevent dropping the packet."

Although Gorti discloses a scheduler coupled to a real-time queue and a non-real-time queue, Gorti fails to cure the noted deficiencies of Ma. Gorti at col. 2, lines 15-

22. And, LaVigne, although it discloses queues 91-95, fails to cure the noted deficiencies of Ma and Gorti.

Moreover, a careful scrutiny of Ma, Gorti, and LaVigne discloses that nowhere do they disclose or suggest the three, separate queues with the features recited in claim 1, such as (1) "at least one arrival queue of a plurality of arrival queues, wherein each of the plurality of arrival queues handles packets based on a traffic class associated with priority;" (2) "placing each packet in the allocated arrival queue if said arrival queue is not full, otherwise dropping said packet;" (3) "placing the packet in the allocated processor queue if said processor queue is not full, wherein the at least one transfer queue and the at least one processor queue do not drop packets, and wherein the scheduler inhibits placement of the packet when the processor queue is full to prevent dropping the packet."

In view of the foregoing, claim 1 is allowable over Ma, Gorti, and LaVigne, whether taken alone or in combination, and the rejection under 35 U.S.C. § 103(a) of claim 1, as well as claims 2-8 and 11-17 at least by reason of their dependency from independent claim 1, should be withdrawn.

Independent claims 2, 35 and 46, although of different scope, include some of the features noted above with respect to claim 1. For at least the reasons noted above, claims 35 and 46 are allowable over Ma, Gorti, and LaVigne,, whether taken alone or in combination, and the rejection under 35 U.S.C. § 103(a) of claims 2, 25 and 46, as well as claims 36-38 and 41-45 at least by reason of their dependency, should be withdrawn.

Regarding the motivation to combine, Applicants submit that the Examiner's proposed combination, which relies on Ma, Gorti, and LaVigne, would impermissibly

change the fundamental principle of operation of those references and likely lead to an inoperative combination. *See* M.P.E.P 2143.03("[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959))." See also *Ex Parte Toftness*, 2008 WL 4451384 (Bd. Pat. App. & Int 2008) (reversing the Examiner's section 103 rejection as the proposed combination would yield an inoperative device). Here, Ma discloses a router that places an input packet at a given receive queue on an given transmit queue based on capacities (described by Ma as the "hungriest" interfaces). Ma clearly has no need for a scheduler or any mechanism for dropping or not dropping packets. Thus, inserting Gorti's scheduler would require a fundamental change to the principle of operation of Ma. Moreover, such insertion would likely lead to an inoperative system for at least the reason that Gorti's scheduler only schedules between a real-time queue and non-real time queue. Therefore, the rejection of the currently pending claims under 35 U.S.C. § 103(a) should be withdrawn for this additional reason.

The Examiner rejected claims 9, 10, 39, and 40 under 35 U.S.C. § 103(a) as unpatentable over Ma, Gorti, LaVigne, and U.S. Patent 6,789,056 to Vinnakota. Applicants respectfully traverse this rejection.

Claims 9 and 10 depend from claim 1 and includes all of the feature recited therein. For at least the reasons noted above with respect to claim 1, neither Ma, Gorti, LaVigne discloses or suggests the above-noted features. Moreover, although Vinnakota discloses a packet processor using digital signal processing, it fails to cure

the deficiencies of Ma, Gorti, LaVigne. Therefore, claims 9, 10, 39, and 40 are allowable over Ma, Gorti, LaVigne, and Vinnakota, whether taken alone or in combination, and the rejection under 35 U.S.C. § 103(a) of claims 9, 10, 39, and 40, should be withdrawn.

CONCLUSION

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

No fees are believed to be due, however the Commissioner is authorized to charge any additional fees or credit overpayments to Deposit Account No. 50-0311, reference No. 39700-638N01US/NC40070US. If there are any questions regarding this reply, the Examiner is encouraged to contact the undersigned at the telephone number provided below.

Respectfully submitted,

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